REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1, 6 through 10, and 12 remain in this case. Claims 2 through 5, 11, and 13 are canceled. Claims 6 and 8 are amended.

The provisional double patenting rejections of claims 1 through 13 are noted. Upon the completion of prosecution of one or more of the applications involved in these rejections, or upon the completion of prosecution of this application if it is the first case to reach allowance, Applicants offer to respond to this issue as appropriate, considering the effect of amendments to the conflicting claims that may be made prior to that time.

In this regard, Applicants have recently responded to an Office Action in copending application S.N. 09/998,330, in which the sole basis of rejection was a nonstatutory double patenting rejection relative to the claims in this case. No amendment was made to the claims in that case. It is therefore expected that application S.N. 09/998,330 will issue prior to the allowance of this application.

In this regard, and to further the prosecution of this application relative to application S.N. 09/998,330, claims 2 through 5, 11, and 13 are canceled from this application. Claim 8, previously dependent on claim 2 (now canceled), is amended to now depend on claim 1, and includes the limitations of original claim 2.

Claims 6 and 7 were rejected under §112, ¶2 as indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. Claim 6 is amended to now refer to a second plurality of processors, and to provide antecedent basis for a new instruction, and to cancel language referring to an old instruction, thus addressing each basis of rejection. The punctuation at the end of claim 6 is also corrected. No new matter is presented by this

amendment to claim 6. Applicants therefore respectfully submit that claims 6 and 7 are in sufficiently definite form as to meet all of the requirements of §112.

Remaining claims 1, 6 through 10, and 12 were rejected under §103 as unpatentable over the Tarui et al. reference[1] in view of the Falik et al. reference[2]. The Examiner asserted that the Tarui et al. reference teaches each elements of independent claim 1, with the exception of a debugging operation, which the Examiner found to be taught by the Falik et al. reference.[3] The Examiner asserted that it would have been obvious for one skilled in the art to have employed the Tarui et al. teachings in debugging a multiple processor system such as taught by Falik et al., and claim 1 was rejected accordingly.[4] The elements presented by dependent claims 6 through 9, and by the other independent claims 10 and 12, were found by the Examiner to be present in one or the other of these two references.[5]

Applicants respectfully traverse the §103 rejection of the claims in this case. Specifically, Applicants submit that the combined teachings of the applied references fall far short of the requirements of independent claims 1, 10, and 12, much less of dependent claims 6 through 9, and that there is no suggestion from the prior art to modify these combined teachings in such a manner as to reach the claims.

Claim 1 in this application is directed to a method of transparently writing to shared memory in the debugging of a multiple processor system. Among other steps, the claimed method requires detecting a write request to a shared memory location by a first debug session associated with a first processor, selecting the first processor to perform the write request if that processor has write access to the shared memory location, and if the first processor does not have write access, searching a software memory map to determine if another second processor has write access to that location, and selecting that second processor if so. The method of claim 1 provides important advantages in the complicated process of debugging a multiple processor

---

[1] U.S. Patent No. 6,088,770, issued July 11, 2000, to Tarui et al.
[2] U.S. Patent No. 6,065,078, issued May 16, 2000, to Falik et al.
[3] Office Action of September 1, 2004, page 5, ¶10.
[4] *Id.*
[5] Office Action, *supra,* pages 7 through 11.

system, primarily by ensuring coherency of shared memory among all the processors in an efficient manner.[6]

In his detailed application of prior art teachings against claim 1, the Examiner asserts that the Tarui et al. reference teaches the determining of whether a first processor has write access to a shared memory location,[7] selecting the first processor to perform the write request if so,[8] if the first processor does not have write access, searching a software memory map to determine if a second processor has write access to that shared memory location[9] and if so, selecting the second processor to perform the write request.[10] Applicants respectfully submit that this application of the Tarui et al. reference is in error, specifically that the reference does not teach what the Examiner alleges that it teaches. Accordingly, Applicants respectfully submit that the rejection of claim 1 and its dependent claims is therefore in error and should be withdrawn.

As evident from the Tarui et al. reference itself, the disclosed system includes multiple "nodes", each including multiple CPUs, part of a main memory, and main memory access circuitry 130.[11] The main memory of this multiple-processor, multiple-node, system includes local portions within each node, and a shared portion within each node to form a "distributed shared memory".[12] The main memory access circuitry 130 at each node includes a "remote decision circuit" 132, which is "a circuit for judging whether an address accessed from the CPU is internal (an address of the main memory included in the particular node) or remote (an address of the main memory possessed by any other node)".[13] In other words, upon a CPU in one of the nodes performing an access of shared memory, the remote decision circuit 132 in that node determines whether the CPU is accessing memory within its own node, or instead

---

[6] Specification of S.N. 09/998,755, pages 2 through 4, ¶¶[05] through [09].
[7] Office Action, *supra,* page 6, *citing* Tarui et al., *supra,* at column 9, lines 42 through 47.
[8] *Id., citing* Tarui et al., *supra,* at column 14, lines 22 through 26.
[9] *Id., citing* Tarui et al., *supra,* at column 9, lines 32 through 41.
[10] *Id., citing* Tarui et al, *supra,* at column 15, lines 46 through 52.
[11] Tarui et al., *supra,* column 6, lines 10 through 17.
[12] *Id.,* at column 6, lines 25 through 33.
[13] *Id.,* at column 6, lines 58 through 62.

accessing shared memory at another node.[14] The reference simply does not disclose any determining of whether a particular processor has "write access" to a shared memory location, and then selecting a processor to effect the operation. Instead, the remote decision circuit 132 of the Tarui et al. reference simply determines whether the memory location is within the same node as the requesting CPU, or is in another node in this multiple node system. In contrast to determining whether a first processor has write access to the shared memory location as claimed, the Tarui et al. reference instead discloses at most the determining of whether the memory location is within the same node as the requesting processor, or is in a different node.

Secondly, the Tarui et al. reference fails to disclose the passing of a write request to a selected second processor for execution, if the first processor does not have write access to the shared memory location. Even assuming, for the sake of argument, that the Tarui et al. reference discloses the determining of whether a first processor has write access to the shared memory location,[15] the reference fails to disclose the passing of a write request to a second processor for execution. Rather, the Tarui et al. reference discloses that a writeback ("WB") command received from another node is carried out by a main memory access circuit "B" (146),[16] and not by another processor. According to the reference, the CPUs at this remote node are simply not involved in the write operation, and are not passed the write request as required by the claim. The Tarui et al. reference therefore simply fails to disclose the passing step required by claim 1, particularly for the case in which the second processor is selected because the first processor does not have write access to the shared memory location, as required by claim 1.

The Falik et al. reference was not cited as providing any teachings regarding these method steps that are missing from the Tarui et al. reference, and indeed it does not provide such teachings. The other prior art of record in this case also lack disclosure of these method steps.

---

[14] *Id.*, at column 9, lines 4 through 11, lines 32 through 47.
[15] Which it does not so disclose, for the reasons mentioned above.
[16] Tarui et al., *supra*, column 17, lines 26 through 34.

Accordingly, Applicants respectfully submit that the combined teachings of the applied references fall short of the requirements of claim 1 and its remaining dependent claims.

Applicants further respectfully submit that there is no suggestion from the prior art to modify the teachings of the Tarui et al. and Falik et al. references, to the extent that the combination of these references is at all suggested, in such a manner as to reach claim 1 and its dependent claims. First, there is simply no mention in the Tarui et al. reference of any debugging operation; rather, the reference is confined to a description of how such a multi-node multi-processor system operates in practice. Secondly, contrary to the assertion of the Examiner, there is no suggestion to use the arrangement of the Tarui et al. reference to perform debugging in the Falik et al. reference. Indeed, there is no multiple-node arrangement in the Falik et al. reference, and it is beyond one's comprehension that one would complicate the Falik et al. system with a multiple-node, multiple-CPU-per-node, system as disclosed by Tarui et al., and as asserted by the Examiner. Furthermore, the difference between the purpose of the operation as disclosed in the Tarui et al. reference (*i.e.*, to provide a system with distributed shared memory) and the purpose of the claimed method (in performing debugging of a multiple processor system) is so substantial that any suggestion to modify the Tarui et al. teachings with the Falik et al. reference, or any of the other prior art of record in this case, is necessarily based on the improper hindsight application of Applicants' own teachings. The important benefits provided by the method of claim 1 further support the patentability of the claim over the applied references.

For these reasons, Applicants respectfully submit that claim 1 and its remaining dependent claims 6 through 9 are patentably distinct over the prior art of record in this case.

Claim 10 is directed to a software development system including a software development tool operable to support debugging of an application program executing on the hardware system, this tool using a method comprising method steps corresponding to those discussed above relative to claim 1. And claim 12 is directed to a digital system, comprised of multiple processors with common shared memory, for executing an application program that

was developed with a software development tool using a method comprising method steps corresponding to those discussed above relative to claim 1.

For the same reasons as discussed above relative to claim 1, Applicants respectfully traverse the §103 rejection of claims 10 and 12, and respectfully submit that claims 10 and 12 are in fact patentably distinct over the applied prior art. Specifically, Applicants submit that neither of the applied references disclose the selecting of a second processor to perform a write request if a first processor does not have write access to a shared memory location, and that neither reference discloses the passing of the write request to the selected second processor for execution, both as required by claims 10 and 12.

As discussed above relative to claim 1, Applicants submit that the Examiner's assertions that the Tarui et al. reference teaches the determining of whether a first processor has write access to a shared memory location,[17] selects the first processor to perform the write request if so,[18] and if the first processor does not have write access, searches a software memory map to determine if a second processor has write access to that shared memory location[19] and if so, selects the second processor to perform the write request,[20] are all in error. Instead, the Tarui et al. reference discloses main memory access circuitry 130 at each of multiple nodes (each node including multiple CPUs) that includes a remote decision circuit for judging whether an address accessed from the CPU is internal to its node, or remote because the address is in memory "possessed by any other node".[21] According to the Tarui et al. reference, the remote decision circuit in a node determines whether the CPU is accessing memory within its own node, or is instead accessing shared memory at another node.[22] According to this reference, there is no determining of whether the CPU has "write access" to a shared memory location, and therefore there is no selecting of a processor to effect the operation. At most, the Tarui et al. reference discloses determining the node in which the addressed memory location (in actuality,

---

[17] Office Action, *supra,* page 6, *citing* Tarui et al., *supra,* at column 9, lines 42 through 47.
[18] *Id., citing* Tarui et al., *supra,* at column 14, lines 22 through 26.
[19] *Id., citing* Tarui et al., *supra,* at column 9, lines 32 through 41.
[20] *Id., citing* Tarui et al, *supra,* at column 15, lines 46 through 52.
[21] *Id.,* at column 6, lines 58 through 62.
[22] *Id.,* at column 9, lines 4 through 11, lines 32 through 47.

determining whether the memory location is at the requesting node, or is in another remote node).

Secondly, the Tarui et al. reference fails to disclose passing a write request to a selected second processor for execution, in the event that a first processor does not have write access to the shared memory location, as required by claims 10 and 12. The Tarui et al. reference instead discloses that a writeback command received from a remote node is carried out by a main memory access circuit in the node containing the shared memory location,[23] but is not disclosed as being carried out by another (selected second) processor, as required by the claim. The Tarui et al. reference therefore simply fails to disclose the passing step of the claims, particularly for the case in which the second processor is selected.

The Falik et al. reference, and the other prior art of record, also lack teachings in this regard.

Accordingly, Applicants respectfully submit that the combined teachings of the applied references fall short of the requirements of claims 10 and 12.

Applicants further respectfully submit that there is no suggestion from the prior art to modify the teachings of the Tarui et al. and Falik et al. references, to the extent that the combination of these references is at all suggested, in such a manner as to reach claims 10 and 12. As urged above, there is no mention in the Tarui et al. reference of any debugging operation, and it is beyond comprehension that the skilled artisan would be motivated to incorporate the complicated multi-node system of the Tarui et al. reference into the debugging system of the Falik et al. reference. Furthermore, only by the improper hindsight use of Applicants' own teachings would one realize that the complicated multi-node distributed shared memory system of the Tarui et al. reference could be further modified to use the presence of absence of write access for a given CPU to shared memory, and to then select and use a second CPU in a different node to perform the otherwise prohibited write access, much less in a debugging method within a software development tool, as required by claims 10 and

---

[23] Tarui et al., *supra*, column 17, lines 26 through 34.

12. For these reasons, Applicants respectfully submit that claims 10 and 12 are patentably distinct over the prior art of record in this case.

The other prior art cited but not applied has been considered but is not felt to come within the scope of the claims in this case.

The undersigned notes the indication by the Examiner that the references cited within the specification have not been specifically considered. Those references are listed on a form PTO/SB/08 submitted with this Amendment, and copies of the references are enclosed.

Applicants further wish to bring the other references indicated on the enclosed form PTO/SB/08 to the attention of the Patent and Trademark Office. Each of these references were cited in an Office Action in copending related application S.N. 09/998,330.

All of the references are in the English language. As such, no additional statement of relevance is provided in this paper.[24] The fee under 37 C.F.R. §1.17(p) is submitted by way of the enclosed Fee Transmittal.

By citing these references, Applicants do not admit that any of these references is, or is considered to be, material to the patentability of any of the claims of this application.[25]

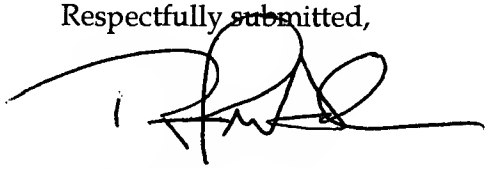
Consideration of this information in the examination of this application is respectfully requested.

---

[24] 37 C.F.R. §1.97(3)(i).
[25] 37 C.F.R. §1.97(h).

For these reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,



Rodney M. Anderson

Registry No. 31,939

Attorney for Applicants

Anderson, Levine & Lintel, L.L.P.

14785 Preston Road, Suite 650

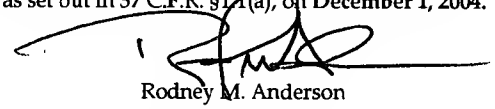
Dallas, Texas 75254

(972) 664-9554

CERTIFICATE OF MAILING

37 C.F.R. 1.8

The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, and addressed as set out in 37 C.F.R. §1.1(a), on **December 1, 2004.**



Rodney M. Anderson

Registry No. 31,939